REGULATING UNUSED/INACTIVE RESOURCES IN PROGRAMMABLE LOGIC DEVICES FOR STATIC POWER REDUCTION

ABSTRACT

A method of operating a programmable logic device, including the steps of using a full V_{DD} supply voltage to operate one or more active blocks of the programmable logic device, and using a reduced supply voltage (e.g., ½ V_{DD}) to operate one or more inactive blocks of the programmable logic device. The full VDD supply voltage and reduced supply voltage can be provided to the blocks of the programmable logic device through high-voltage n-channel transistors. A boosted voltage, greater than VDD, is applied to the gate of an n-channel transistor to provide the full VDD supply voltage to an active block. A standby voltage, less than VDD, is applied to the gate of an n-channel transistor to provide the reduced supply voltage to an inactive block. The inactive blocks can be determined during run time and/or design time of the programmable logic device.